

Prepared		Product Specifications AN17821A	Ref No.	A
Checked			Total Page	9
Approved			Page No.	1

Structure	Silicon Monolithic Bipolar IC
Appearance	SIL-12 Pin Plastic Package (Power Type with Fin)
Application	Low Frequency Amplifier
Function	BTL 5.0W x 2ch Power Amplifier with Standby Function and Volume Function

A	Absolute Maximum Ratings				
No.	Item	Symbol	Ratings	Unit	Note
1	Storage Temperature	Tstg	-55 ~ +150	° C	1
2	Operating Ambient Temperature	Topr	-25 ~ +70	° C	1
3	Operating Ambient Pressure	Popr	1.013x10 ⁵ ±0.61x10 ⁵	Pa	
4	Operating Constant Acceleration	Gopr	9,810	m/s ²	
5	Operating Shock	Sopr	4,900	m/s ²	
6	Supply Voltage	Vcc	14.4	V	2
7	Supply Current	Icc	2.0	A	
8	Power Dissipation	P _D	1.92	W	Ta=70°C

Operating Supply Voltage Range	Vcc	3.5V ~ 13.5V
--------------------------------	-----	--------------

Note 1) The temperature of all items shall be Ta=25°C except storage temperature and operating ambient temperature.

2) At no signal input.

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
06-MAR-2002				

Prepared		Product Specifications AN17821A	Ref No.	B-1
Checked			Total Page	9
Approved			Page No.	2

B		Electrical Characteristics (Unless otherwise specified, the ambient temperature is 25°C±2°C, Vcc=8.0V, frequency=1kHz and RL=8Ω.)							
No	Item	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					min	typ	max		
1	Quiescent Circuit Current	ICQ	1	Vin=0V, Vol=0V	-	45	100	mA	
2	Standby Current	ISTB	1	Vin=0V, Vol=0V	-	1	10	μA	
3	Output Noise Voltage	VNO	1	Rg=10kΩ, Vol=0V	-	0.10	0.4	mVrms	1
4	Voltage Gain	GV	1	Po=0.5W, Vol=1.25V	31	33	35	dB	
5	Total Harmonic Distortion	THD	1	Po=0.5W, Vol=1.25V	-	0.10	0.5	%	
6	Maximum Power Output 1	PO1	1	THD=10%, Vol=1.25V	2.4	3.0	-	W	
7	Maximum Power Output 2	PO2	1	Vcc=11V THD=10%, Vol=1.25V	4.0	5.0	-	W	
8	Ripple Rejection Ratio	RR	1	Rg=10kΩ, Vol=0V Vr=0.5Vrms, fr=120Hz	30	50	-	dB	1
9	Output Offset Voltage	Voff	1	Rg=10kΩ, Vol=0V	-250	0	250	mV	
10	Volume Attenuation Ratio	Att	1	Po=0.5W, Vol=0V	70	85	-	dB	1
11	Channel Balance 1	CB1	1	Po=0.5W, Vol=1.25V	-1	0	1	dB	
12	Channel Balance 2	CB2	1	Po=0.5W, Vol=0.6V	-2	0	2	dB	
13	Middle Voltage Gain	GVm	1	Po=0.5W, Vol=0.6V	20.5	23.5	26.5	dB	
14	Channel Crosstalk	CT	1	Po=0.5W, Vol=1.25V	40	55	-	dB	

Note 1) For this measurement, use the BPF = 15Hz ~ 30kHz (12dB/OCT).

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
06-MAR-2002				

Prepared		Product Specifications (Reference Data for Design) AN17821A	Ref No.	B-2
Checked			Total Page	9
Approved			Page No.	3

No	Item	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					min	typ	max		
1	Standby pin current	ISTB2	1	V _{in} =0V, V _{STB} =3V	-	-	25	μA	
2	Volume pin current	I _{VOL}	1	V _{in} =0V, V _{ol} =0V	-12	-	-	μA	
3	Input Impedance	Z _i	1	V _{in} =±0.3V _{DC}	24	30	36	kΩ	

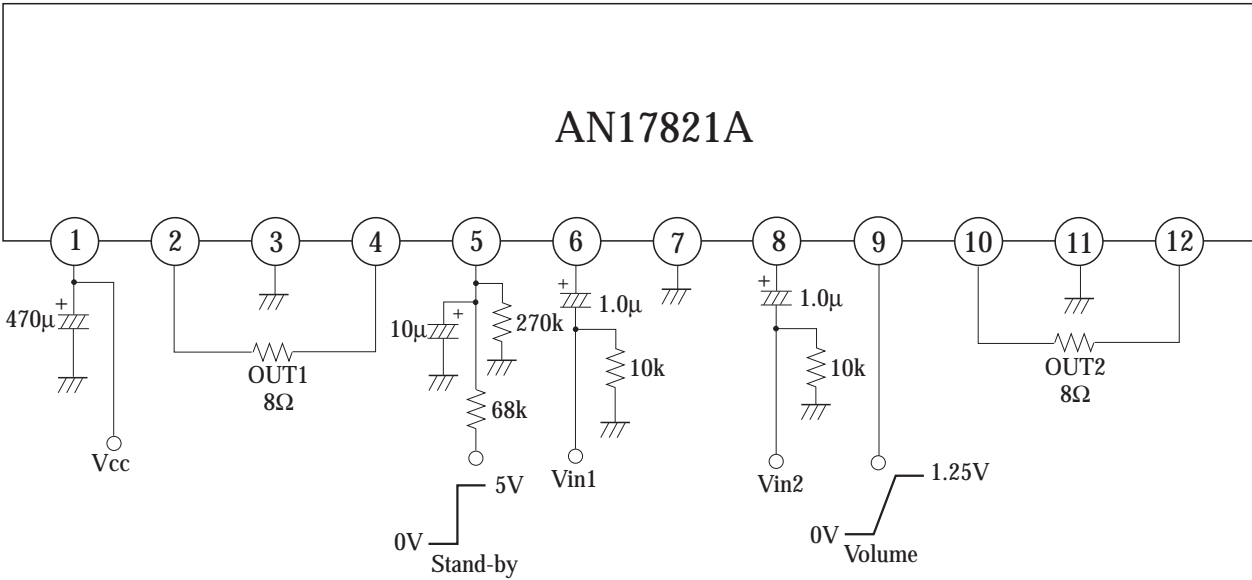
Note) The above characteristics are reference values determined for IC design, but not guaranteed values for shipping inspection. If problems were to occur, counter measures will be sincerely discussed.

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
06-MAR-2002				

Prepared		Product Specifications AN17821A	Ref No.	C
Checked			Total Page	9
Approved			Page No.	4

(Description of test circuit and test method)

Test Circuit 1

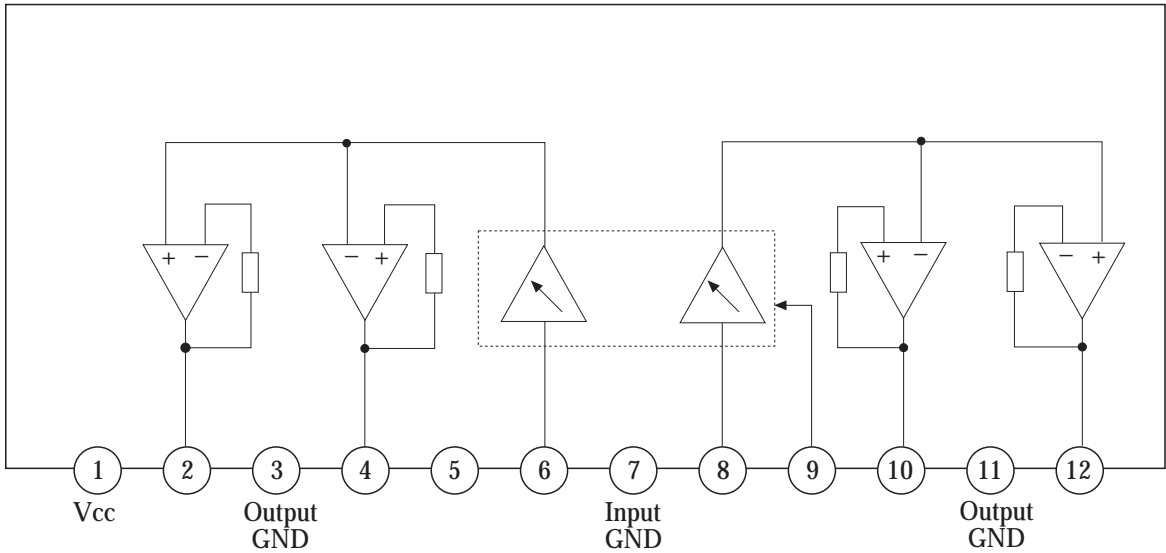


Note) If the standby pin is open or 0V, the IC is on standby state.
The IC is in the state of volume minimum if the Volume pin is ground.
The IC is in the state of volume maximum if the Volume pin is open.

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
06-MAR-2002				

Prepared		Product Specifications AN17821A	Ref No.	D
Checked			Total Page	9
Approved			Page No.	5

Circuit Function Block Diagram



Pin Descriptions

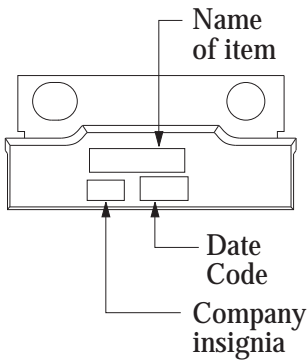
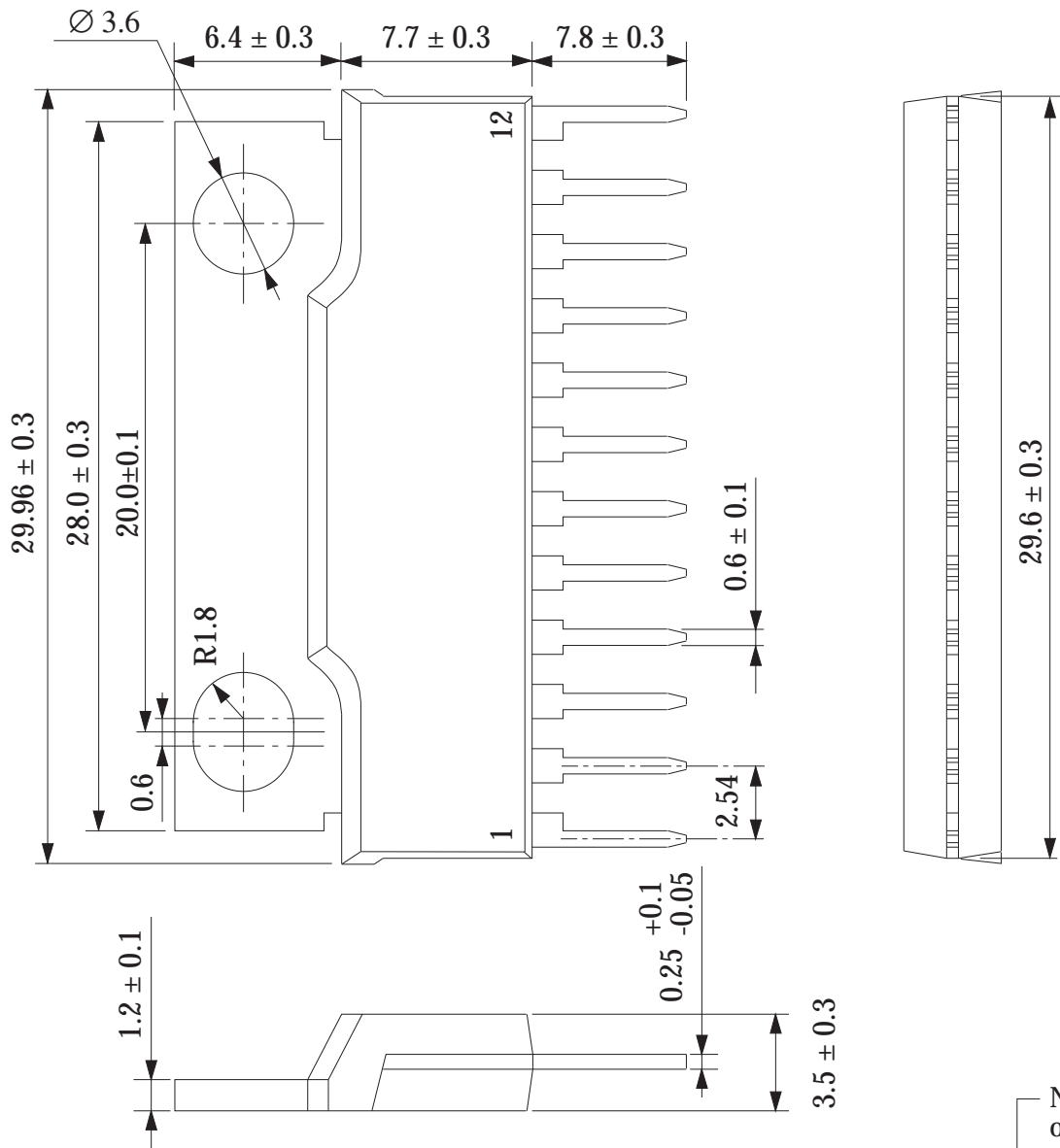
Pin No.	Description	Pin No.	Description
1	Vcc	7	GND (Input)
2	Ch.1 Output (+)	8	Ch.2 Input
3	GND (Ch.1 Output)	9	Volume
4	Ch.1 Output (-)	10	Ch.2 Output (-)
5	Standby	11	GND (Ch.2 Output)
6	Ch.1 Input	12	Ch.2 Output (+)

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
06-MAR-2002				

Prepared		Product Specifications AN17821A	Ref No.	E
Checked			Total Page	9
Approved			Page No.	6

Package Name	FP-12S
--------------	--------

Unit : mm



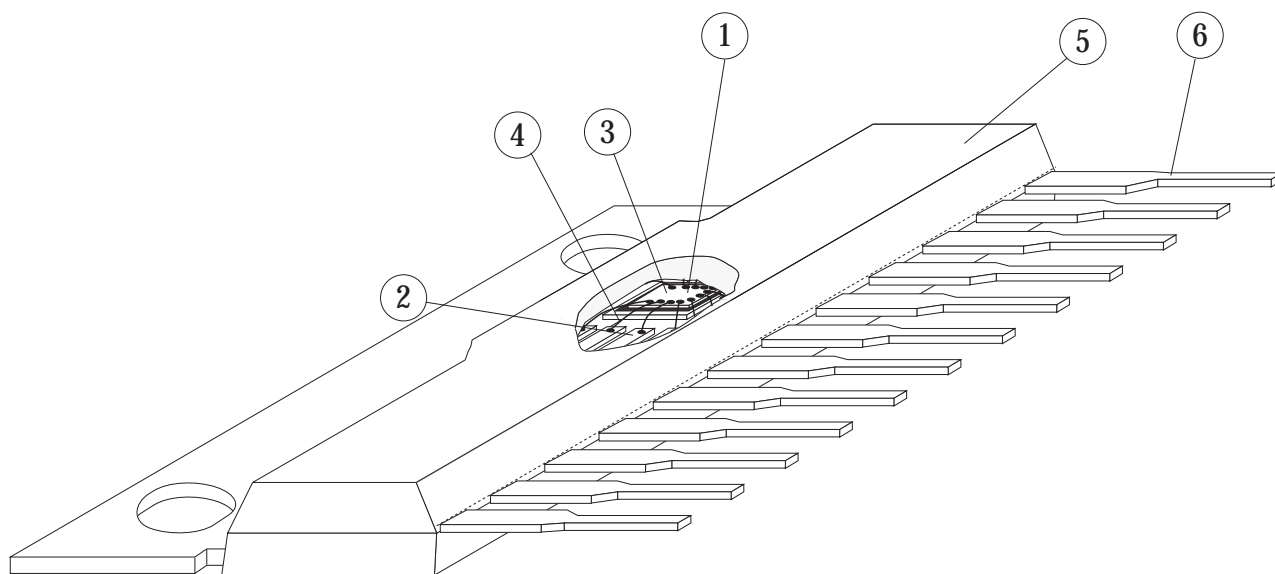
Eff. Date	Eff. Date	Eff. Date	Eff. Date	
06-MAR-2002				

Prepared		Product Specifications AN17821A	Ref No.	F
Checked			Total Page	9
Approved			Page No.	7

(Structure Description)

Chip surface passivation	SiN,	PSG,	Others ()	①
Lead frame material	Fe group,	Cu group,	Others ()	②, ⑥
Inner lead surface process	Ag plating,	Au plating,	Others ()	②
Outer lead surface process	Solder plating,	Solder dip,	Others ()	⑥
Chip mounting method	Ag paste,	Au-Si alloy,	Solder, Others ()	③
Wire bonding method	Thermalsonic bonding,		Others ()	④
Mold material	Epoxy,		Others ()	⑤
Molding method	Transfer mold,	Multiplunger mold,	Others ()	⑤
Fin material	Cu Group		Others ()	⑦

Package FP-12S

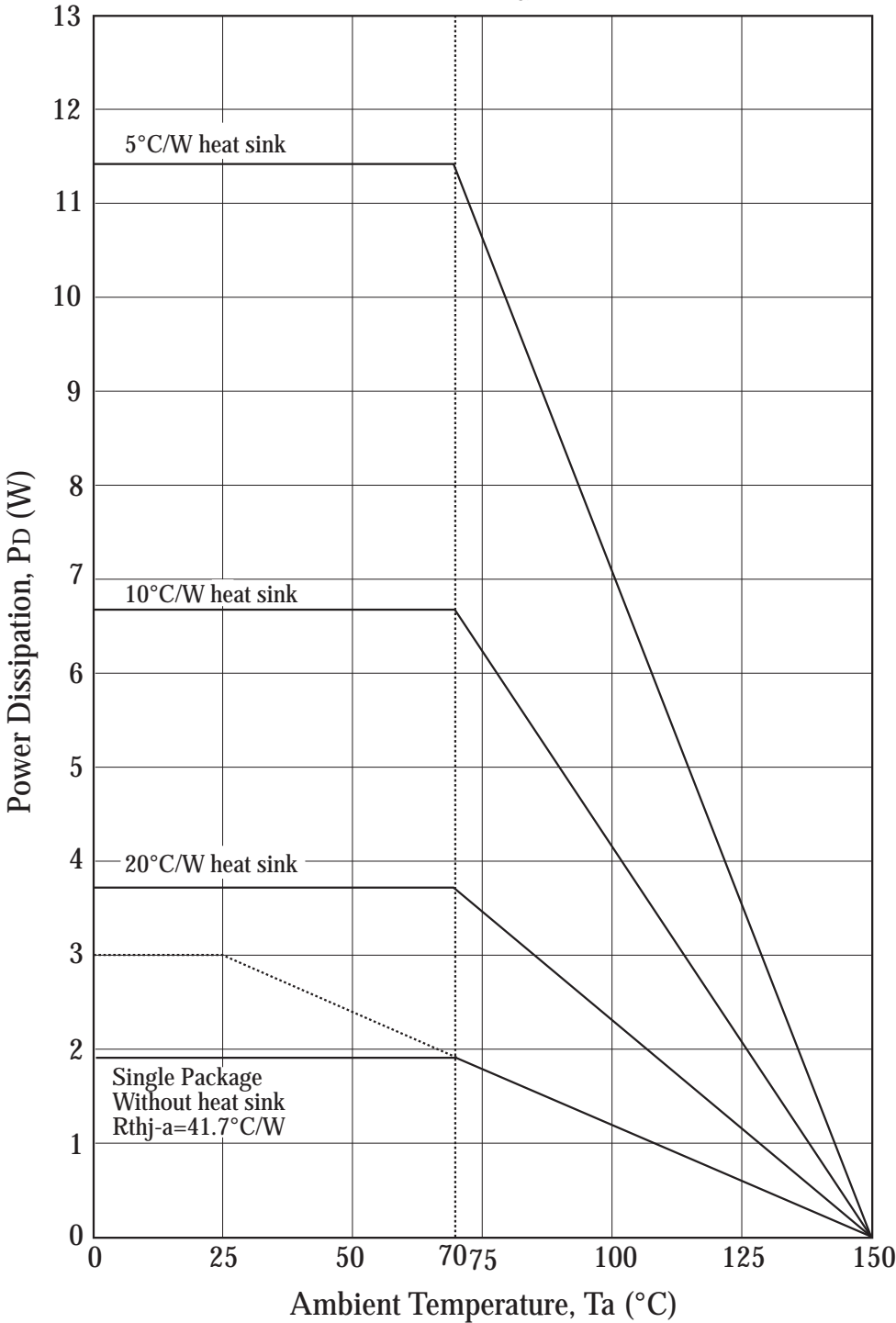


Eff. Date	Eff. Date	Eff. Date	Eff. Date	
06-MAR-2002				

Prepared		Product Specifications (Technical Data) AN17821A	Ref No.	G
Checked			Total Page	9
Approved			Page No.	8

$$\left(\begin{array}{l} R_{th(j-c)} = 2^{\circ}\text{C/W} \\ R_{th(j-a)} = 41.7^{\circ}\text{C/W} \end{array} \right)$$

FP-12S Package Power Dissipation
PD - Ta



Eff. Date	Eff. Date	Eff. Date	Eff. Date	
06-MAR-2002				

Prepared		Product Specifications (Technical Data) AN17821A	Ref No.	G
Checked			Total Page	9
Approved			Page No.	9

(Precautions for use)

- 1) Make sure that the IC is free of any pin short-circuiting, ground short-circuiting, pin shift and reverse insertion.
- 2) Ground the radiation fin so that there will be no difference in electric potential between the radiation fin and ground.
- 3) The thermal protection circuit operates at a Tj of approximately 150°C. The thermal protection circuit is reset automatically when the temperature drops.
- 4) Make sure that the heat radiation design is effective enough if the Vcc is comparatively high or the IC operates high output power.
- 5) Connect only ground pin for signal sources to the signal GND pin of the amplifier on the previous stage.

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
06-MAR-2002				